



UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Kao et al.
Serial No: 09/256,265
Filing Date: February 23, 1999
Title: "METHOD AND APPARATUS FOR SPLIT GATE SOURCE SIDE
INJECTION FLASH MEMORY CELL AND ARRAY WITH
DEDICATED ERASE GATES"

Docket No: 16405-0311
Group Art Unit: 2815
Examiner: Diaz, J.

Box RCE
Assistant Commissioner for Patents
Washington, D.C. 20231

#22/E
12-30-02
Payton

**REQUEST FOR CONTINUED EXAMINATION (RCE)
UNDER 37 CFR 1.114 AND
AMENDMENT**

Sir:

This Amendment is submitted in response to the Final Office Action mailed on September 19, 2002, relating to the above-identified application. Applicants respectfully request reconsideration of the patent application in light of the following remarks. Please amend the above-identified application as follows:

In the Claims:

1. (Amended) A semiconductor device having at least one transistor, the device comprising:
a substrate having a channel region defined thereon;
a first insulating layer disposed over said channel region and over at least a portion of said substrate;
a floating gate having at least a substantial portion thereof disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;
a second insulating layer disposed over said side walls and over said top surface of said floating gate;
a control gate having a first portion disposed over a portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first